Simulation of Daisy Chain Flip-Chip interconnections

M. Fretz[1], G. Spinola Durante*[1]
[1]CSEM SA, Central Switzerland Center, Untere Gründlistrasse 1, CH-6055 Alpnach Dorf, Switzerland
Corresponding author:* gsd@csem.ch

Abstract: Flip-chip interconnection technologies have been tested through the use of a test chip with embedded single-bump daisy chains.

The Flip-Chip technologies are selected among Au bump thermocompression (TC) with and without NCA underfiller, anisotropic conductive adhesive (ACA) bonding, and AuSn20 eutectic solder. The single bumps were then measured with a high precision resistance meter and compared between them to check the electrical behavior of different interconnection technologies.

Simulation with Comsol helped to provide a more accurate estimation of the bump resistance, calculating a correction factor to the classical 4-probe measurement scheme expectations. This correction factor was also experimentally measured and is mainly caused by current and voltage path asymmetries arising from the bump routing layout and its 3D geometrical features. The FEM model allowed normalizing results for measured resistances among different pads within the same daisy chain chip.

Keywords: daisy chain, flip-chip, bonding, ACA, eutectic, AuSn, thermocompression,

1. Introduction

Flip-chip interconnections are becoming more and more interesting to industry since face-down electrical and mechanical connection of electronic components (ICs, MEMS) allows shrinking of assembly footprint, when compared to conventional die-attach and wire-bonding approach. The flip-chip interconnects resistance is usually tested through the use of daisy chain chips. The aim of these test structures is to probe the average electrical resistance that will clearly depend on the chosen Flip-chip technology.

In this paper the selected Flip-chip technologies are gold thermo-compression (TC) bonding with and without NCA underfiller, anisotropic conductive adhesive (ACA), and AuSn20 eutectic solder [1]. The flip chip single-bump daisy chains are assembled and then measured with a high precision resistance meter. Results are compared to check for different electrical behavior among the selected interconnection technologies. The adopted measurement setup is the classical 4-probe measurement scheme.

Comsol simulation provided a more accurate estimation of the expected single bump resistance for each contact in the daisy chain layout. According to experiments the measured bump resistance can change as much as a factor ~2 due to a layout 3D asymmetry effect.

The model allows normalizing results among the chips and within chips, since it accounts for variations in resistance among different pads. This effect is called current crowding effect and it's basically a current and voltage path asymmetry due to the 3D geometry of the model with both in-plane and out of plane current flows and 90° current flow turns.

The 3D FEM model has been checked and simplified in several ways including the following aspects:

- calibration of routing metal conductivity with experimental data
- impact of different routing metal thicknesses
- extrapolation to routing metal of 1um thickness
- calculation of the resistance correction factor in both negligible and finite bump resistance

2. Daisy chain experimental results

2.1 Daisy chain layout description

In order to characterize flip chip bonding techniques, two distinct substrate and chip layouts with appropriate metal structures were designed for measuring electrical resistances of single bumps in a daisy chain fashion. Figure 1 shows the metal structures of the chips and the substrates. The substrate provides larger landing pads at the peripherals which can be contacted by probe needles.

The design comprises sites for flip chip contacts depicted with circles in figure 2. It can be either a gold stud bump or AuSn solder bump assembly or equivalently a bonding surface with average properties given by ACA particles. The

metallization of the chip is designed in a way that it electrically connects all bumps.

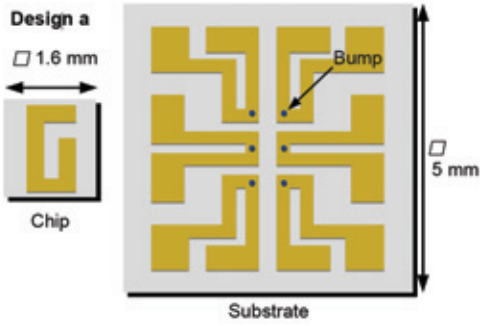

Figure 1. Test device for measuring electrical resistances of single bumps

It allows determination of the resistance of the four bumps, labeled with 1,2,3, and 4 on the left side in figure 2.

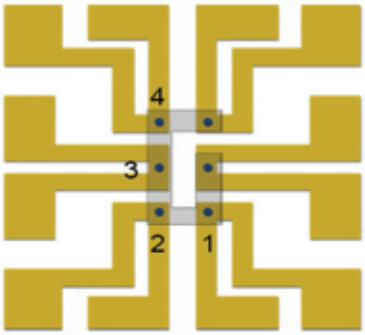

Figure 2. Overlaid metal structures of chip and substrate. The hatched shapes depict the chip metallisation.

2.2 Flip chip bonding approaches

The thermocompression bonding process is described in fig. 3 both for thermocompression with stud bumps (branch "a") and for bonding with non-conductive adhesive and stud bumps (branch "b"). The second process is precisely spoken not a thermo-compression process. The third process consists of AuSn20 solder process which is the most used solder in the field of optoelectronic packaging. It allows fluxless and Pb-free soldering of Au pads at relatively high temperatures. It provides a hard bond and shows no creep. The solder is electrodeposited in circular holes with 80um in diameter. In the subsequent reflow process, the solder forms a 40µm high half-sphere, protruding over the substrate. Figure 4 shows the developed bonding process with solder bumps, carried out in atmosphere. First, chip and substrate are aligned in the flip chip bonder FC150. Then the parts are assembled.

Finally the ACA-bonding process is sketched in figure 5. It is similar to the bonding process with non-conductive adhesive apart from the flattening of the stud bumps.

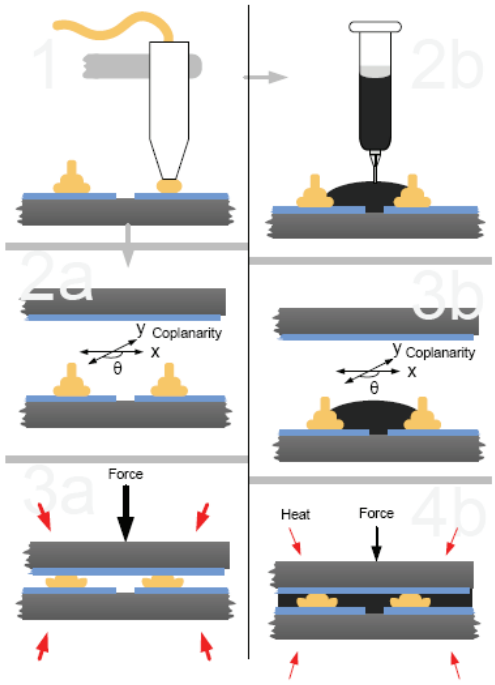

Figure 3. Process steps for thermocompression with gold studs. Branch a (left) depicts the standard thermocompression process. The alignment step (2a) is followed by the thermocompression process (3a). bonding with nonconductive adhesive (branch b) first requires a dispensing step (2b). Then chip and substrate are aligned (3b) and bonded (4b).

The advantage of ACA process over other bonding processes is the small bonding force per bump is sufficient. Such small forces are not strong enough to squeeze unflattened bumps in the bonding process. Reliable contacts with small and uniform electrical resistances are thus only achieved with flattened bumps.

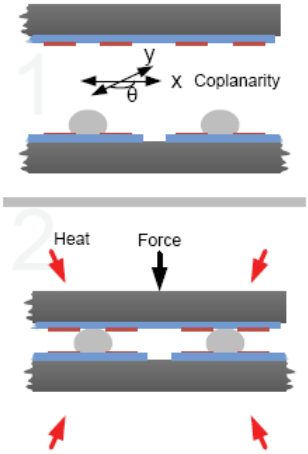

Figure 4. Process steps for bonding with eutectic AuSn20 solder: Chip and substrate have to be aligned (1). Then they are bonded by increasing the temperature above the melting point of the solder and by applying moderate force (2). The force supports wetting of the chip pads.

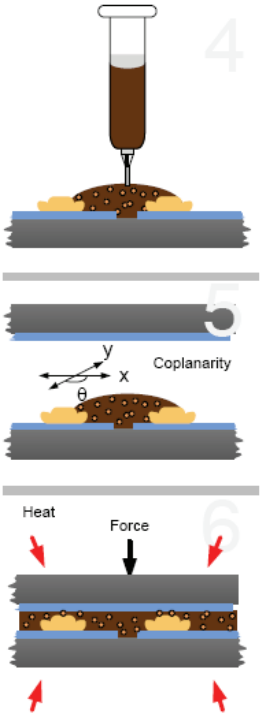

Figure 5. Process steps for ACA bonding. Gold studs are placed with a commercial wire bonder and flattened (1-3). Dispensing of the ACA (4), alignment of chip and substrate (5), and bonding (6) is carried out with the flip chip bonder FC150.

2.3 Daisy chain measurement method

Single bump resistance measurements require an accurate measurement unit and a dedicated setup. A Keithley 2750 Multimeter with an input impedance of 10 MOhm was used. Usually, a so-called 4-point or 4-wire configuration is set up in order to measure low resistances (see figure 6). A current is driven through the resistance R_{Bump} which has to be measured. In a 2-point configuration the voltage drop across the measurement unit would be measured. The ratio voltage drop/current is identified as the resistance in question (assuming ohmic behavior of all components). But the voltage drop along the wires and across the contacts between wires and device is included in the measurement. Hence, the calculated resistance value is overestimated. In a 4-wire configuration the contribution of the wires and the contacts can be avoided. The measured resistance comprises the resistance of the investigated element ($R_{Element}$) and the resistances (R_{Lines}) of the lines between contacts and element.

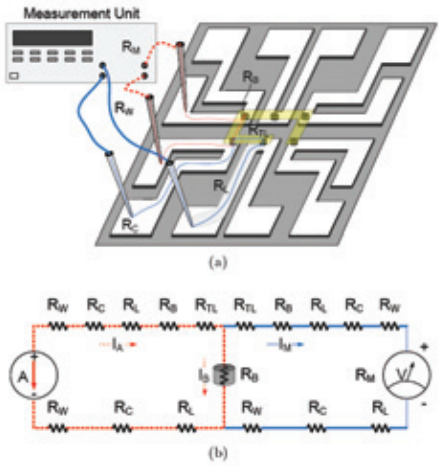

Figure 6. 4-Point measurement principle. The contributing resistances (a) and the circuit schematic (b) are illustrated. The dashed red lines depict the electrical circuit providing the driving current, whereas the solid blue lines depict the voltage-measurement circuit.

The displayed resistance value $R_{Measure}$ is given by the voltage across the measurement unit divided by the induced current:

$$R_{Measure} = U_M / I_A$$

whereas the true resistance is given by the fraction of voltage across the interconnect bump and current through this bump.
Estimating the contributing resistances of the setup (see table 1), it can be shown that R_B and $R_{Measure}$ are related by the following approximation:
$R_B \sim R_{Measure} \cdot (1 + 4 \cdot 10^{-7})$

The error induced by the measurement setup is therefore negligible. The uncertainty of the measurement is given by the accuracy of the measurement unit. To set a typical limit, we observe when measuring ~10mΩ in 4-probes mode a standard deviation <0.1mΩ.

- R_W: Connection wires 1Ω
- R_C: Probe-to-metal-line contact 1 Ω
- R_L: Bottom substrate metal line 100 mΩ
- R_{TL}: Top die metal line 20 mΩ
- R_B: Interconnect bump 10 mΩ
- R_M: Measurement unit 10 MΩ

Table 1. Relevant resistances in the 4-point setup included in figure 6.

2.4 Daisy chain measurement results

For each flip chip bonding procedure at least eight devices with 6 (of which 4 can be measured) bumps were assembled. 10 devices were assembled with ACA. Each bump was measured as described in section 2.3 and according to the location of bumps as labeled in figure 2. The values are graphically presented in figure 7. One column is the averaged resistance value of one bonding site for a specific bonding procedure. The values were not averaged over all bonding sites because site three shows a significantly lower contact resistance than the other sites. Even though a 4-point measurement was done, the resistance of site three is by a factor of ~2 lower than the resistances of the other three sites.

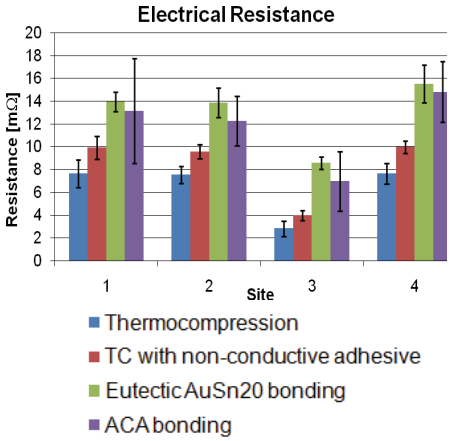

Figure 7: Electrical resistance for the investigated flip chip bonding processes. The averaged resistance for each site is measured and plotted with the standard deviation.

The metal structure and the measurement geometry influence the measurement, as depicted in figure 8. In the upper drawing the electrical current flows through the right side of the top electrode, and then goes down along the bump, and through the bottom electrode on the right side. In the bottom drawing the current flows through the bottom electrode on the left side. It can be seen that in the upper case the current crowds along the right edge of the bump, whereas in the lower case the current density is lower. The upper case is known to cause current crowding effects at the electrode-bump interface [2].

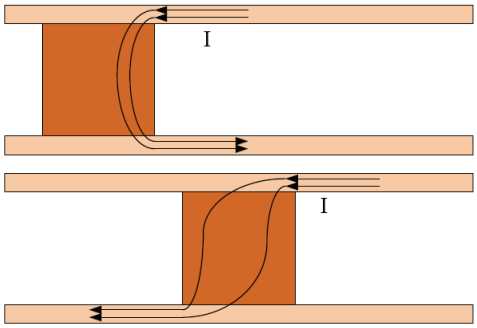

Figure 8: Influence of measurement geometry on measured resistance value of a flip chip interconnection.

Current crowding strongly depends on the geometry of the flip chip interconnections. It is

the most important reason that accounts for the differences of the contact resistances of the bonding sites because the current is restricted to a small portion of the cross section of the bump.

According to Ohm's law, the resistance is inversely proportional to the cross-sectional area of a conductor. It can be seen from figure 7 that thermocompression with gold studs provides the lowest contact resistance, and soldering with eutectic AuSn20 the highest contact resistance. But it is important to understand that the resistance values for the different flip chip bonding techniques are to be compared with care. Specifically the final bump height and width, and contact resistances are crucial for defining the bump resistance. In table 2 a summary comparison is shown to better appreciate the measured resistance differences.

- TC: 80um diameter, ~20um height
- Eutectic: 80um diameter, ~30um height
- ACA: 80um diameter, ~25um height

Table 2. Relevant geometrical data of the interconnection bumps realized

3. Numerical method

3.1 FEM model in Comsol

The model is built importing the 2D gds (electronic cad format) file and extruded in 3D. The mesh is fairly dense as can be seen from figure 9, since the structure has a very high aspect ratio. In fact the model has typical features of ~1um up to ~20um thicknesses and ~mm wide structures leading to ~50:1 up to ~1000:1 aspect-ratios. The final model that can be seen in figure 10 was solved with ~3.5MDOF.

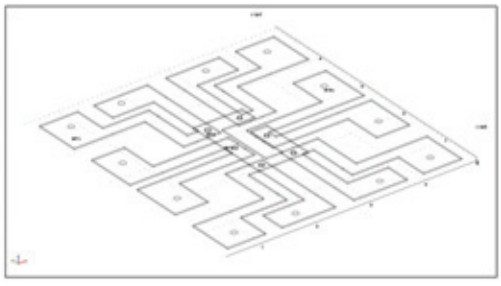

Figure 9: Extruded 3D model from gds ecad file

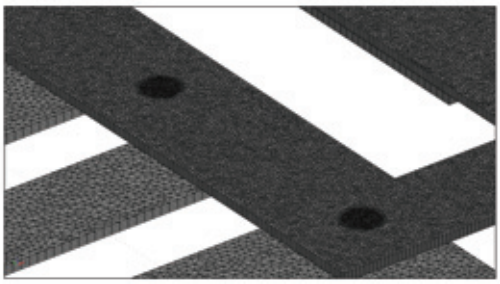

Figure 10: Zoom on meshed 3D model

3.2 FEM model conductivity calibration

To calibrate the conductivity coefficient of the routing metal layer, a 4-point measurement of two neighboring Au pads has been performed. The measurement led to 347mOhm pad-pad resistance. The material conductivity has then been matched to achieve 0.347V Voltage drop across the pads as indicated in figure 11, when imposing 1A current flow.

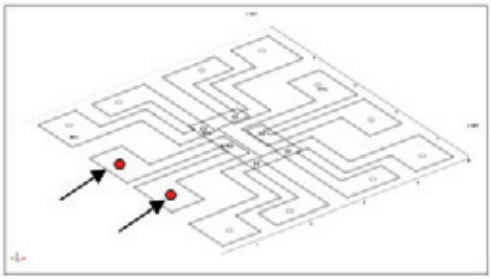

Figure 11: Metal line conductivity FEM calibration

3.3 FEM model thickness approximation

To deal with the very high aspect ratios a strong approximation has been chosen, while still leaving the model in 3D geometry: the current is flowing in-plane along the routing metals (almost) everywhere. Thus the routing metals have been chosen of 20um thickness, rescaling the conductivity to match the equivalent in-plane resistance of 1um thickness as measured in section 3.2. This strong approximation will be fully justified in section 3.5. The bumps are typically chosen with different heights: 20um for TC, ACA and 30um for AuSn solder bump. The bump heights, in the contrary to the routing metals, are chosen to be realistic values.

3.4 Method to extract bump resistance

The FEM model is solved using a static AC/DC simulation, imposing 1A on the blue pad and fixing ground condition on the red pad as can be seen in figure 12. The Site 1 (see fig. 6) bump resistance is read checking the voltage drop on the connecting pads (see red line on figure 12) and the corresponding plot in figure 13 shows that there are roughly 7.7mΩ between these two pads which is in agreement with measured data (fig.7, [1]).

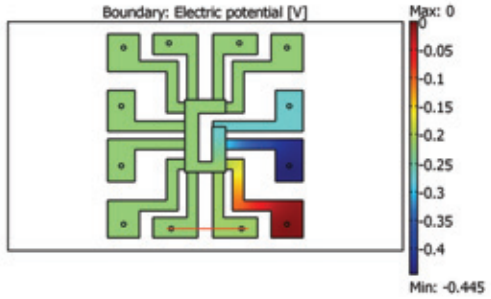

Figure 12: Site 1 simulation, TC case

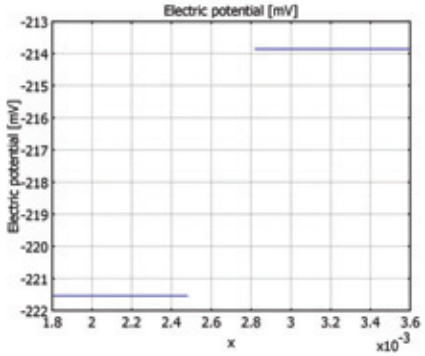

Figure 13: Line cross-section plot for site 1, TC case

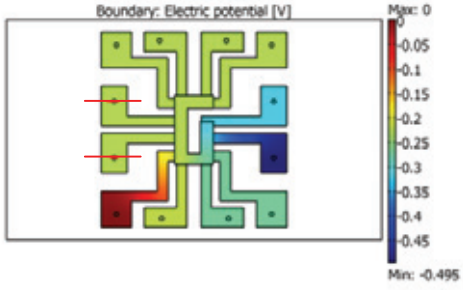

Figure 14: Site 3 simulation, TC case

In figure 14 is shown the simulation result for Site 3 (TC) and we can extract with a similar procedure as described previously the bump resistance of 3.4mΩ. The measured value is ~2.8mΩ (see fig.7).

The results appear quite satisfactory since the difference from simulation and measured data is anyway within the standard deviation of the measurement as can be seen for Site 3, case TC, in figure 7.

3.5 Extrapolation of results to 1um thick routing metal

Different thickness cases have been simulated to check the impact of routing metal thickness. The trend is parabolic and has an asymptote within the standard deviation of the measured resistance for site 3 (see fig. 15). Site 3 (TC) was chosen as a reference since here the layout influence is stronger. It can be also inferred from this result that 20um thickness can be used as a reasonable value to perform all the simulations.

The current crowding effect is of course stronger the higher the ratio between bump thickness and routing metal thickness as expected.

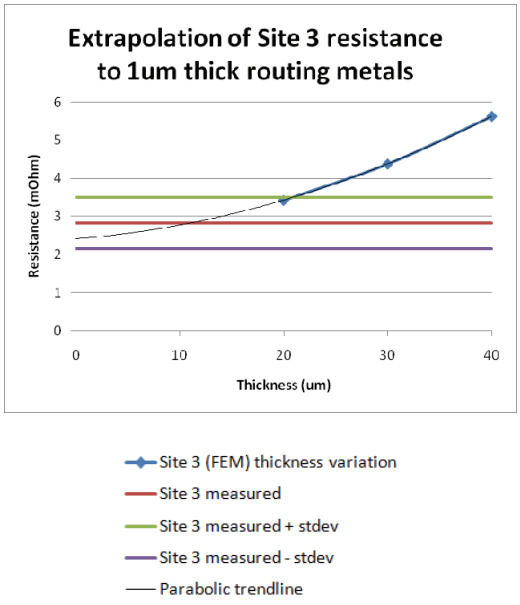

Figure 15: Impact of different routing thickness on site 3 simulated resistance, TC case.

3.6 Calculation of the resistance correction factor in both negligible and finite bump resistance cases

There is still an important point to be mentioned, before summarizing the complete results: in all 3 cases TC, TC with underfiller and ACA bonding, the bump height is in the range of ~20-25 um and simulation results yield similar ratios for site1/site3 resistances. If we consider a gold bump of 80um diameter and 20um high, the equivalent vertical resistance is ~0.09mΩ, which is in fact much smaller than the measured and simulated values. The reason is clearly that we are measuring the daisy chain routing paths, since the bump itself is too small to contribute significantly. Each layer will contribute with its own contact resistance. It is interesting to note that in the case of eutectic solder bonding the resistance is quite higher, and this cannot be explained even if we consider a bump of 30um height. The increase of resistance of the bump is hidden, in the multi-layer formation in the AuSn complex soldering metallurgy.

4. Simulation results

To fully exploit and assess the simulation results it was decided to rescale the measured data according to simulated ratios for (site n.1 / site n.X) resistances. In all cases we have chosen 20um routing metal thickness and bump high is always 20um high except for AuSn bump which is ~30um high. In the case of AuSn bump its resistivity has also been rescaled to match the measured resistance in site 1 (solder) of ~14mΩ.

5. Simulation and experiment comparison

In figure 16 are summarized the rescaled measured values according to (site n.1 / site n.X) ratios calculated with Comsol. For all bonding technologies the rescaled site resistance values appear to have average values close to site 1, almost within the standard deviation of each individual set of measurements. This is a clear indication that the current crowding effect has been correctly taken into account, even with the chosen strong approximations on the metal routing thickness and the bump simplified geometry and simplified layer structure.

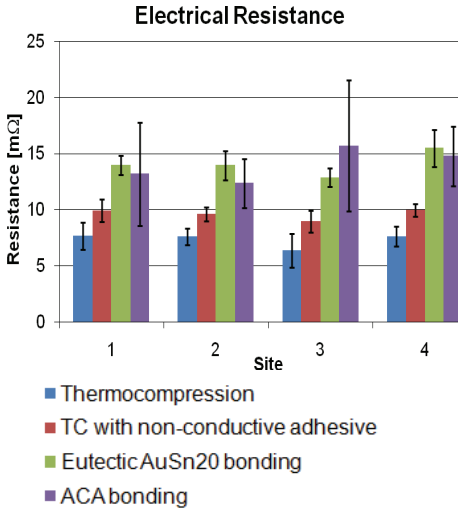

Figure 16: rescaled measured values, according to the ratios calculated with Comsol.

6. Conclusions

This type of simulation shows that we can model 3D effects with Comsol and try to catch the essence of measured phenomena even when dealing with approximation assumptions. The prediction of FEM helps to understand the measured values and to normalize the resistance results. The impact is clearly to improve the design of interconnects and also to allow more accurate bump comparison for future reliability assessment.

7. References

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8. Acknowledgements

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