

Finite Element Analysis of Integrated Circuit Interconnect Lines on Lossy Silicon Substrate

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Abstract: The silicon substrate has a significant effect on the inductance parameter of a lossy interconnect line on integrated circuit. It is essential to take this into account in determining the transmission line electrical parameters. In this paper, a new quasi-TEM capacitance and inductance analysis of multiconductor multilayer interconnects is successfully demonstrated using finite element method (FEM). We specifically illustrate the electrostatic modeling of single and coupled interconnected lines on a silicon-silicon oxide substrate. Also, we determine the quasi-static spectral for the potential distribution of the silicon-integrated circuit.

Keywords: Finite element method, capacitance, inductance, interconnect, silicon substrate.

1. Introduction

Due to complexity of electromagnetic modeling, researchers and scientists always look for development of accurate and fast methods to extract the parameters of electronic interconnects and package structures. In recent years, we have observed a magnificent application and development in the complexity, density, and speed of operations of integrated circuits (ICs), multichip modules (MCMs), and printed circuit-board (PCB). For examples, MCMs are extensively used to reduce interconnection delay and crosstalk effects in complex electronic systems. Multiconductor transmission lines embedded in multilayered dielectric media are known as the basic interconnection units in ICs and MCMs, and have been characterized with the distributed circuit parameters such as capacitance C and inductance L matrices under quasi-TEM conditions. Also, these distributed circuit parameters are very important factor in the electrical behavior and performance of other microwave integrated circuits (MIC) and very

large scale integration (VLSI) chips. Today, in the advances for fabrication of high speed integrated circuits, it is essential to examine the limitations due to the parasitic coupled mechanisms preset in silicon-integrated circuit processes. To optimize electrical properties of IC interconnects such as minimization of the length of the interconnection lines, an adequate attention must be given to the geometrical size of their transverse cross sections; the estimation of the transmission line parameters requires being accurate for system design.

Multiconductor multilayered structures are essential for ICs, MCMs, and PCB systems, due to the important effects on the transmission characteristics of high-speed signals. Also, the transmission lines effect on the IC interconnects become extremely important for the transmission behavior of interconnect lines on silicon oxide-silicon semiconducting substrate. The conducting silicon substrate causes capacitive and inductive coupling effects in the structure. Therefore, in this work, we apply the finite element method (FEM) for parameter extraction for electrostatic modeling of single and coupled interconnects lines on silicon-silicon oxide substrate.

Many researchers have presented various kinds of methods for solving the problem. These include equivalent source and measured equation of dielectric Green's function and boundary integral equation approach [1-4], CAD and quasi-static spectral domain [5-8], complex image method [9-10], quasi-stationary full-wave analysis and Fourier integral transformation [11], and conformal mapping method [12]. We illustrate that our method using FEM is suitable and effective as other methods for modeling of inhomogeneous quasistatic multiconductor interconnects in multilayered dielectric media.

In this work, we design of single and coupled interconnect lines on silicon-silicon oxide substrate using FEM. We focus on the calculation of the capacitance per unit length and inductance per unit length matrices of the single and coupled interconnects lines on silicon-silicon oxide substrate and we determine the quasi-static spectral for the potential distribution of the silicon-integrated circuit.

2. Results and Discussions

The models are designed in 2D using electrostatic environment in order to compare our results with some other available methods. In the boundary condition of the model's design, we use ground boundary which is zero potential ($V = 0$) for the shield. We use port condition for the conductors to force the potential or current to one or zero depending on the setting.

We use FEM in our computations because it is suitable for the computation of electromagnetic fields in strongly inhomogeneous media and it has high computation accuracy and fast computation speed.

In the following subsections, we demonstrate our work on modeling of the single and coupled interconnects lines on silicon-silicon oxide substrate and we determine the quasi-static spectral for the potential distribution of the silicon-integrated circuit.

Our computation is focused on calculating calculation of the capacitance per unit length and inductance per unit length matrices of the transmission line interconnects on silicon-silicon oxide (Si-SiO₂) substrate.

2.1 Single Interconnect Line on Si-SiO₂ Substrate

In this section, we illustrate the modeling of Single interconnect line on silicon-silicon oxide substrate by focusing only on the calculation of the capacitance per unit length and inductance per unit length. Figure 1 shows the geometry of the model.

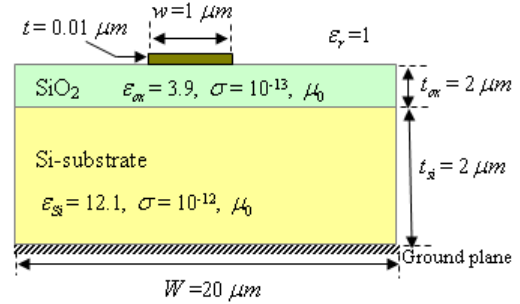


Figure 1. Cross-section of single interconnects line on silicon-silicon oxide substrate.

The single line capacitance (C_s) per unit length placed on a stacked layer of the oxide and bulk silicon is given [13]:

$$C_s = \epsilon_{ox} \left\{ 1.15 \left(\frac{w}{t_{ox}} \right) + 1.40 \left(\frac{t}{t_{ox}} \right)^{0.222} \left(2 + \frac{2w}{W} \right) + 4.12 \left(\frac{t}{t_{ox}} \right)^{0.728} \left(\frac{t_{ox}}{W} \right) \right\} \quad (1)$$

where $\epsilon_{ox} = 3.9 \times 8.855 \times 10^{-14}$ (F/cm), w = width of the single conductor, t = thickness of the single conductor, W = width of the silicon-silicon oxide substrate, t = thickness of the single conductor, t_{ox} = thickness of SiO₂ layer .

The value of the single line capacitance (C_s) using eq. 1 is 5.33×10^{-11} F/m; furthermore, using our method the value of C_s is 4.43×10^{-11} F/m.

For lossless or low dielectric substrates, the single line inductance per unit length (L_s) can be directly and commonly computed from the equation 2 [14]:

$$L_s = \frac{\mu_0 \epsilon_0}{C_0} \quad , \quad (2)$$

where ϵ_0 = permittivity of free space

$= \frac{1}{36\pi} \times 10^{-9} = 8.854 \times 10^{-12}$ F/m, μ_0 = permeability of free space or vacuum = $4 \pi \times 10^{-7} = 12.6 \times 10^{-7}$ H/m, L_s = inductance of the single transmission line, C_0 = the capacitance of the single transmission line when all dielectric constants are set equal to 1.

On the other hand, equation (2) is not accurate enough to be used for lossy lines, because the silicon substrate has high conductivity which effect results in the slow wave mode appears when the signal frequency is not so high and the resistivity of the S_i substrate is moderate. In that mode, the storage of electric and magnetic energies is spatially separated. As a result, the integrated circuit (IC) interconnect model without the S_i semiconducting effect cannot be accepted for today's high-performance very large scale integration (VLSI) circuit designs any more [1].

Therefore, the inductance (L_s) model of a single interconnect line on silicon substrate is given by [15]:

$$L_s = \frac{\mu_0}{2\pi} \ln \left[\left(\frac{t_{ox} + t_{si}}{0.59w} + 1.1 \right) - 0.5 + \sqrt{\left(\frac{t_{ox} + t_{si}}{0.59w} + 1.1 \right)^2 - 1.05} \right] \quad (3)$$

where μ_0 = permeability of free space or vacuum = $4 \pi \times 10^{-7} = 12.6 \times 10^{-7}$ H/m, t_{si} = thickness of S_i layer (substrate). Using equation (3) of the results for $L_s = 1.488 \mu H$

Table 1 shows the comparison results for the inductance per unit length (L_s) of the structure when the single interconnects line on silicon-silicon oxide substrate.

Table 1 Values of inductance per unit length (in μ H/m) for the single interconnects line on silicon-silicon oxide substrate

Single line inductance per unit length (L_s)	Approach [1]	Experiment [16]	Equation 3
L_s	1.305	1.2505	1.488

Furthermore, Figures 2 through 4 show the potential distribution of the model with their variations in spectra peaks and full width half maximum (FWHM) from $(x,y) = (0,502 \mu m)$ to $(x,y) = (20 \mu m, 502 \mu m)$, from $(x,y) = (0,500 \mu m)$ to $(x,y) = (20 \mu m, 502 \mu m)$, from $(x,y) = (0,0)$ to $(x,y) = (20 \mu m, 1500 \mu m)$, and from $(x,y) = (0,0)$ to $(x,y) = (20 \mu m, 1500 \mu m)$, respectively.

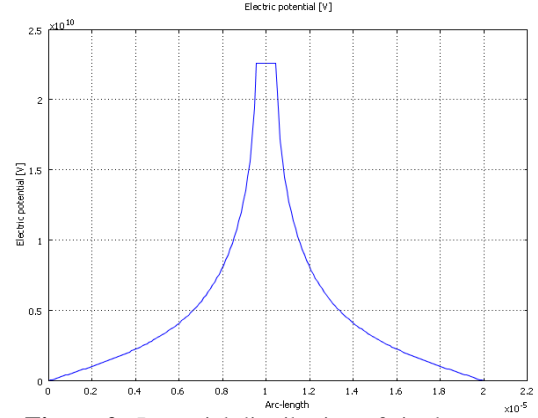


Figure 2. Potential distribution of single interconnects line on silicon-silicon oxide substrate from $(x,y) = (0,502 \mu m)$ to $(x,y) = (20 \mu m, 502 \mu m)$.

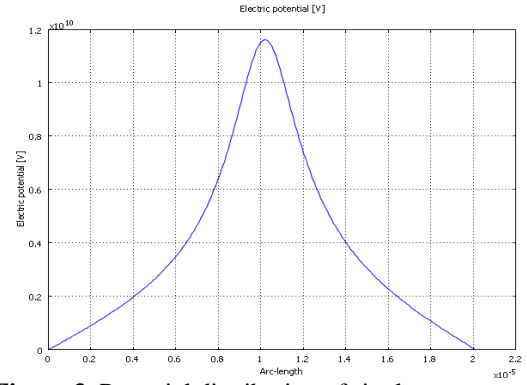


Figure 3. Potential distribution of single interconnects line on silicon-silicon oxide substrate from $(x,y) = (0,500 \mu m)$ to $(x,y) = (20 \mu m, 502 \mu m)$.

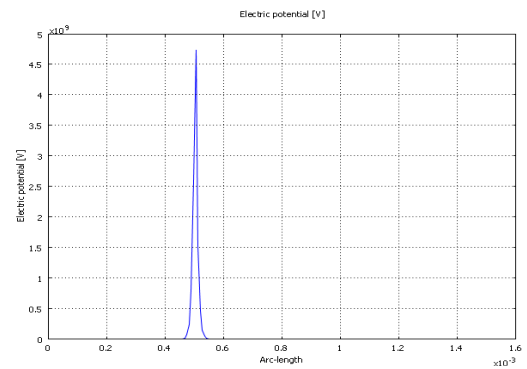


Figure 4. Potential distribution of single interconnects line on silicon-silicon oxide substrate from $(x,y) = (0,0)$ to $(x,y) = (20 \mu m, 1500 \mu m)$.

2.2 Coupled Interconnect Lines on Si-SiO₂ Substrate

In this section, we demonstrate the electrostatic modeling of coupled interconnect lines on silicon-silicon oxide substrate by focusing only on the calculation of the inductance per unit length matrix. Figure 5 shows the geometry of the model with the parameters values.

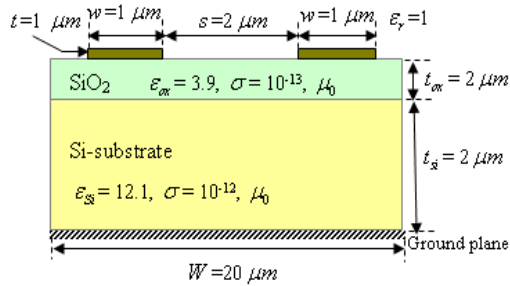


Figure 5. Cross-section of coupled interconnect lines on silicon-silicon oxide substrate.

We use the results of our computation of capacitance to find inductance matrix.

The inductance $[L]$ and capacitance per unit

length $[C]$ of multiconductor transmission lines system are commonly related for lossless or low lossy lines as [14]

$$[L] = \mu_o \epsilon_o [C_o]^{-1}, \quad (4)$$

where

ϵ_o = permittivity of free space

$$= \frac{1}{36\pi} \times 10^{-9} = 8.854 \times 10^{-12} \text{ F/m}$$

μ_o = permeability of free space or vacuum = $4\pi \times 10^{-7} = 12.6 \times 10^{-7} \text{ H/m}$

$[L]$ = inductance matrix.

$[C_o]^{-1}$ = the inverse matrix of the capacitance of the multiconductor transmission line when all dielectric constants are set equal to 1.

But, the silicon substrate lossy effect must be taken into account to calculate $[L]$ by using the effective dielectric constant μ_{reff} in equation (4) [1]:

$$\mu_{\text{reff}} = \frac{C_s L_s}{\mu_o \epsilon_o}, \quad \text{and} \quad (5)$$

$$[L] = \mu_o \epsilon_o \mu_{\text{reff}} [C_o]^{-1}. \quad (6)$$

Table 2 shows the comparison results for the self and mutual inductances of the structure when the coupled interconnect lines on silicon-silicon oxide substrate.

Table 2 Values of inductance matrix (in $\mu \text{ H/m}$) coefficients for the coupled interconnect lines on silicon-silicon oxide substrate

Inductance matrix ($L_{ij} = L_{ji}$) and L_{ii}	Approach [1]	Our Work
Self inductance, $L_{11} = L_{22}$	1.877	1.841
Mutual inductance, $L_{12} = L_{21}$	0.278	0.253

Base on the table 2, we observe that FEM with Comsol is accurate and efficient for the model in estimating the coupled transmission line parameters of interconnects. The results are compared with the previous work and found to be in good agreement.

Additionally, Figures 6 through 8 show the potential distribution of the model with their variations in spectra peaks and full width half maximum (FWHM), from $(x,y) = (0,502 \mu\text{m})$ to $(x,y) = (20 \mu\text{m}, 502 \mu\text{m})$, from $(x,y) = (0,500 \mu\text{m})$ to $(x,y) = (20 \mu\text{m}, 502 \mu\text{m})$, and from $(x,y) = (0,0)$ to $(x,y) = (20 \mu\text{m}, 1500 \mu\text{m})$, respectively.

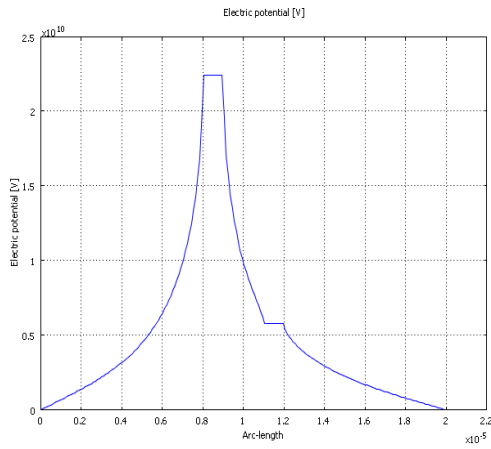


Figure 6. Potential distribution of coupled interconnect lines on silicon-silicon oxide substrate from $(x,y) = (0,502 \mu m)$ to $(x,y) = (20 \mu m, 502 \mu m)$.

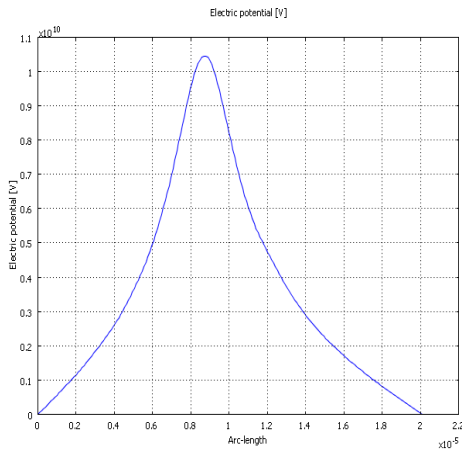


Figure 7. Potential distribution of coupled interconnects line on silicon-silicon oxide substrate from $(x,y) = (0,500 \mu m)$ to $(x,y) = (20 \mu m, 502 \mu m)$.

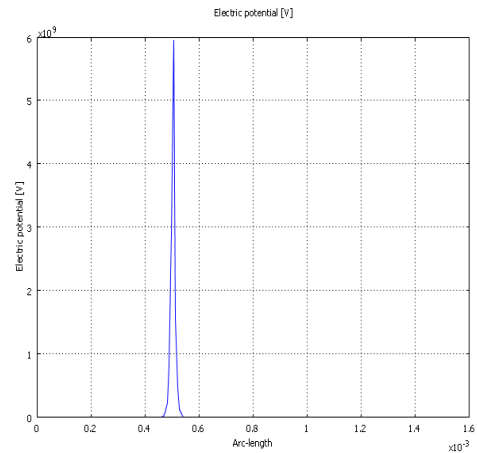


Figure 8. Potential distribution of coupled interconnect lines on silicon-silicon oxide substrate from $(x,y) = (0,0)$ to $(x,y) = (20 \mu m, 1500 \mu m)$.

3. Conclusions

In this article, we have presented the modeling of single and coupled interconnected lines on a silicon-silicon oxide substrate. The results obtained using COMSOL for the capacitance per unit length, and inductance per unit length agree well with those found in the literature. In addition, we obtained for the models the potential distribution.

4. References

1. H. Ymeri, B. Nauwelaers, and K. Maex, "On the modeling of multiconductor multilayer systems for interconnect applications," *Microelectronics Journal*, vol. 32, pp. 351-355, 2001.
2. H. Ymeri, B. Nauwelaers, and K. Maex, "On the frequency-dependent line admittance of VLSI interconnect lines on silicon-based semiconductor substrate," *Microelectronics Journal*, vol. 33, pp. 449-458, 2002.
3. H. Ymeri, B. Nauwelaers, and K. Maex, "On the capacitance and conductance calculations of integrated-circuit interconnects with thick conductors," *Microwave and Optical Technology Letters*, vol. 30, no. 5, pp. 335-339, 2001.

4. W. Delbare and D. De Zutter, "Accurate calculations of the capacitance matrix of a multiconductor transmission line in a multilayered dielectric medium", *IEEE Microwave Symposium Digest*, Long Beach, CA, pp. 1013-1016, 1989.
5. J. Zhang, Y-C. Hahm, V. K. Tripathi, and A. Weisshaar, "CAD-oriented equipment-circuit modeling of on-chip interconnects on lossy silicon substrate," *IEEE Transaction on Microwave Theory and Techniques*, vol. 48, no. 9, pp. 1443-1451, 2000.
6. H. Ymeri, B. Nauwelaers, and K. Maex, "Distributed inductance and resistance per-unit-length formulas for VLSI interconnects on silicon substrate," *Microwave and Optical Technology Letters*, vol. 30, no. 5, pp. 302-304, 2001.
7. H. Ymeri, B. Nauwelaers, K. Maex, S. Vandenberghe, and D. D. Roest, "A CAD-oriented analytical model for frequency-dependent series resistance and inductance of microstrip on-chip interconnects on multilayer silicon substrates," *IEEE Transaction on Advanced Packaging*, vol. 27, no. 1, pp. 126-134, 2004.
8. E. Groteluschen. L. S. Dutta, and S. Zaage. "Full-wave analysis and analytical formulas for the line parameters of transmission lines on semiconductor substrates," *Integration, the VLSI Journal*, vol. 16, pp. 33-58, 1993.
9. C-N. Chiu, "Closed-form expressions for the line-coupling parameters of coupled on-chip interconnects on lossy silicon substrate," *Microwave and Optical Technology Letters*, vol. 43, no. 6, pp. 495-498, 2004.
10. J.J. Yang, G. E. Howard, and Y.L. Chow, "Complex image method for analyzing multiconductor transmission lines in multilayered dielectric media", *International Symposium Digest of Antennas and Propagation*, pp. 862-865, 1991.
11. H. Ymeri, B. Nauwelaers, and K. Maex, "Frequency-dependent mutual resistance and inductance formulas for coupled IC interconnects on an Si-SiO₂ substrate," *Integration, the VLSI Journal*, vol. 30, pp. 133-141, 2001.
12. E. Chen and S. Y. Chou, "Characteristics of coplanar transmission lines multilayer substrates: modeling and experiments," *IEEE Transaction on Microwave Theory and Techniques*, vol. 45, no. 6, pp. 939-945, 1997.
13. T. Sakurai and K. Tamaru, "Simple formulas for two- and three-dimensional capacitances," *IEEE Transactions on Electron Devices*, vol. 30, no. 2, pp. 183-185, 1983.
14. S. M. Musa and M. N. O. Sadiku, "Using Finite Element Method to Calculate Capacitance, Inductance, Characteristic Impedance of Open Microstrip Lines," *Microwave and Optical Technology Letters*, vol. 50, no. 3, pp. 611-614, 2008.
15. Y. Eo and W. R. Eisenstadt, "High-speed VLSI interconnect modeling based on S-parameter measurements," *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, vol. 16, no. 5, pp. 555-562, 1993.
16. W. Jin, H. Yoo, Y. Eo, "Nonuniform multilayer IC interconnect transmission line characterization for fast signal transient simulation of high speed/high density VLSI circuit," *IEICE Transaction on Electronics*, vol. 82, pp. 955-966, 1999.